

Customer No.: 31561  
Application No.: 10/605,306  
Docket No.: 11516-US-PA

# IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:
  - providing a substrate;
  - forming a plurality of conductive structures over the substrate, wherein each conductive structure comprises a conductive layer and a cap layer over the conductive layer;
  - forming spacers on ~~the~~ sidewalls of the conductive structures;
  - forming a first dielectric layer over the substrate;
  - removing a portion of the first dielectric layer, a portion of the cap layer and a portion of the spacers between neighboring conductive structures to form a plurality of first openings;
  - forming a liner layer over a bottom and sidewalls of the first openings;
  - forming a bottom plug over the liner layer in the first openings;
  - forming a second dielectric layer over the substrate;
  - forming a plurality of second openings in the second dielectric layer, wherein each second opening exposes a portion of the bottom plug, and the second opening has a critical dimension smaller than the ~~open end of the~~ first opening;
  - forming a top plug inside the second openings; and
  - forming a plurality of wire lines over the second dielectric layer so that the wire lines and the top plugs are electrically connected.

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2. (original) The method of claim 1, wherein the first opening has a funnel shape.

3. (currently amended) The method of claim 2, wherein the step of forming a the funnel shape opening comprises performing an anisotropic etching operation to remove a portion of the first dielectric layer, a portion of the cap layer and a portion of the spacers between neighboring conductive structures, moreover, the anisotropic etching process uses an etchant with a high etching selectivity between the first dielectric layer and the cap layer/the spacers, a low etching rate for the cap layer/spacer layer but a high etching rate for the first dielectric layer.

**Claim 4 (canceled).**

5. (currently amended) The method of claim 4 1, wherein the step of forming a the liner layer on the bottom and the sidewalls of the first openings comprises:

forming a liner material layer over the substrate to cover the first dielectric layer, the conductive structures and the sidewalls and bottom ~~section~~ of the first openings; and performing an anisotropic etching of the liner material layer to form the liner layer on the sidewalls of the first openings.

6. (original) The method of claim 5, wherein material constituting the liner material layer is different from the second dielectric layer.

**Claim 7 (canceled).**

8. (original) The method of claim 1, wherein the step for forming the top plugs and the wire lines further comprises:

forming a second conductive layer over the substrate to cover the second dielectric layer and fill the second openings, wherein the second conductive layer

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within the second openings form the top plug; and

patterning the second conductive layer to form the wire lines.

9. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate;

forming a plurality of conductive structures over the substrate, wherein each conductive structure comprises a conductive layer and a cap layer over the conductive layer;

forming spacers on ~~the~~ sidewalls of the conductive structures;

forming a dielectric layer over the substrate;

removing a portion of the dielectric layer, a portion of the cap layer and a portion of the spacers between neighboring conductive structures to form a plurality of openings that exposes a shoulder section of the conductive layers;

removing the shoulder section of the conductive layers to form a shoulder recess;

forming a liner layer on ~~the~~ bottom and sidewalls of the openings; and

forming a conductive plug over the liner layer inside the openings.

10. (original) The method of claim 9, wherein the opening has a funnel shape.

11. (currently amended) The method of claim 10, wherein the step of forming a the funnel shape opening comprises performing an anisotropic etching operation to remove a portion of the dielectric layer, a portion of the cap layer and a portion of the spacers between ~~neighboring~~ the conductive structures, moreover, the anisotropic etching process uses an etchant with a high etching selectivity between the dielectric

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layer and the cap layer/the spacers, a low etching rate for the cap layer/spacer layer but a high etching rate for the dielectric layer.

12. (currently amended) The method of claim 9, wherein the step of forming a the liner layer on the sidewalls of the openings comprises:

forming a liner material layer over the substrate to cover the dielectric layer, the conductive structures and the sidewalls and bottom section of the openings; and

performing an anisotropic etching of the liner material layer to form a liner layer on the sidewalls of the openings.

13. (original) The method of claim 12, wherein material constituting the liner material layer is different from the dielectric layer.

**Claims 14-19 (canceled).**

20. (new) A method of manufacturing a conductive plug over a substrate, the substrate comprising a plurality of conductive structures formed thereon, wherein each conductive structure comprises a conductive layer, a cap layer over the conductive layer and spacers on sidewalls thereof, the method comprising:

forming a first dielectric layer over the substrate;

forming a plurality of first openings between the conductive structures, wherein a recess is formed on sidewalls of the first openings proximate to a shoulder of the conductive structures;

forming a liner layer over a bottom and sidewalls of the first openings;

forming a bottom plug over the liner layer in the first openings;

forming a second dielectric layer over the substrate;

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forming a plurality of second openings in the second dielectric layer, wherein each second opening exposes a portion of the bottom plug;

forming a top plug inside the second openings; and

forming a plurality of wire lines over the second dielectric layer so that the wire lines and the top plugs are electrically connected.